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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,241	01/14/2004	Han-Ping Pu	60568 (71987)	4373

7590 08/04/2005

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EXAMINER	
TANG, MINH NHUT	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,241	PU, HAN-PING	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sano (U.S.P. 5,559,446).

As to claim 1, Sano discloses, in Figs. 1 and 2, a wafer test method, comprising the steps of: providing a wafer (W) integrally formed of a plurality of chips (IC chips), each of the chips (IC chips) having an active surface and an opposite inactive surface, with a plurality of bond pads (electrode pads) formed on the active surface; preparing a conductive interposer (2 with wiring substrate 3 for forming conductive layers) composed of a plurality of interposer units (i.e., part corresponding to each IC chip) each corresponding to one of the chips (IC chips), each of the interposer units having a first surface (i.e., upper surface) and an opposite second surface (i.e., lower surface), wherein the first surface (upper surface) of each of the interposer units is formed with a plurality of test pads (i.e., upper ends of through holes 22, hereinafter pads), and the second surface (lower surface) of each of the interposer units is formed with a plurality of test bumps (41) electrically connected to the test pads (pads), the test bumps (41) corresponding to the bond pads (electrode pads) of the chips (IC chips), and mounting the conductive interposer (2) on the wafer (W) such that the test bumps (41) are in

electrical contact with the bond pads (electrode pads) to electrically connect the conductive interposer (2) to the chips (IC chips); and using test probes (51) to contact the test pads (pads) of the conductive interposer (2) to perform tests for the chips (IC chips) of the wafer (W).

As to claim 3, Sano discloses in Figs. 1 and 2, edges of the conductive interposer (2) are supported by a frame (13) that abuts against the wafer (W) to position the conductive interposer (2) on the wafer (W).

As to claim 4, Sano discloses in Fig. 2, the conductive interposer (2) comprises a core (20) having the first surface (upper surface) and the second surface (lower surface), a plurality of conductive traces (31, 42) formed on the first surface (upper surface) and the second surface (lower surface) of the core (20), and a plurality of conductive vias (21, 22) penetrating the core (20) for electrically connecting the conductive traces (31, 42) on the first and second surfaces of the core (20).

As to claim 5, Sano discloses in column 3, line 67, the core (20) is a thin film.

As to claim 6, Sano discloses in column 4, lines 1-5, the core (20) is a substrate made of an organic material.

As to claim 7, Sano discloses in column 3, line 67 to column 4, line 5, the organic material is selected from the group consisting of epoxy resin, polyimide resin, BT (bismaleimide triazine) resin, and FR4 resin.

As to claim 8, Sano discloses in column 4, lines 22-23, the conductive traces (31, 42) are made of copper.

As to claim 9, Sano discloses in Fig. 2, the conductive vias (21, 22) are formed by plating copper in a plurality of through holes penetrating the core (20).

As to claim 10, Sano discloses in Fig. 2, a solder mask (i.e., part of wiring substrate 3) is applied over the first surface (upper surface) of the core (20) and formed with a plurality of openings for exposing predetermined portions of the conductive traces (31), and the exposed portions serve as the test pads (pads).

As to claim 11, Sano discloses in Fig.2, a solder mask (i.e., part of thin substrate 4) is applied over the second surface (lower surface) of the core (20) and formed with a plurality of openings for exposing predetermined portions of the conductive traces (42), allowing the test bumps (41) to be bonded to the exposed portions.

As to claim 12, Sano discloses in Fig. 2, the test bumps (41) are electrically connected to the test pads (pads) by the corresponding conductive traces (31, 42) and conductive vias (21, 22).

As to claim 13, Sano discloses in Fig. 2, the test bumps (41) are electrically connected and redistributed to the test pads (pads) by the corresponding conductive traces (31, 42) and conductive vias (21, 22).

As to claim 14, Sano discloses in column 4, line 11, the test bumps (41) are made of gold.

Response to Arguments

3. Applicant's arguments filed on June 07, 2005 have been fully considered but they are not persuasive.

Applicant, in the Remarks page 9, asserted that the Sano reference does not teach or suggest a wafer test method in which a plurality of interposer units correspond to a plurality of chips, respectively, and wherein each interposer units includes a plurality of test pads electrically connected to bond pads of a chip. The Examiner disagrees because, as disclosed, for example, in column 4, lines 7-10 of the Sano reference, the bumps 41 of the interposer 2 are arranged in corresponding positional relationship with respect to all the electrode pads of the IC chips, so as to be simultaneously brought into contact with the electrode pads of all the IC chips formed on the wafer W. Furthermore, one ordinary skill in the art would recognize that the wafer has a plurality of chips formed thereon, and those chips are separated from each other by scribe lines or lanes. Therefore, for simultaneously contacting a plurality of bump 41 with a plurality of corresponding pads of all the chips formed on the wafer W, it is believed that the interposer 2 would be composed of a plurality of interposer units, each corresponding to each of the chips, separated by scribe lines or lanes, formed on the wafer.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kohno et al. 6,614,246 Probe Structure.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor R. Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MINH NHUT TANG
PRIMARY EXAMINER
8/02/05